

Application No. 10/814,246

Reply to Office Action of May 27, 2005

IN THE ABSTRACT OF THE DISCLOSURE

Page 20, lines 1-22, delete in their entirety and substitute therefore the following new
Abstract of the Disclosure on the next page 5 of this paper.

ABSTRACT

An injection enhanced gate transistor includes a drift layer, a collector layer and a base layer divided into main cell regions and dummy cell regions by a plurality of trenches formed to extend from the top surface of the base layer into the drift layer. The main cell has a first emitter layer selectively formed in the surface layer of the base layer, gate electrodes formed in the trenches, and an emitter electrode located over the base layer. The dummy cell has a second emitter layer selectively formed so as to be scattered in the surface layer of the base layer and have a surface area smaller than that of the first emitter layer to prevent waveform vibration associate with negative gate capacitance.